

ADVANCED SEMICONDUCTOR PACKAGE/WAFER RELIABILITY

Semiconductor reliability is at a crossroads. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. Analysis and experimentation is now performed at the wafer level instead of the packaging level. This requires knowledge of subjects like: design of experiments, testing, technology, processing, materials science, chemistry, and customer expectations. While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate. Your industry needs competent engineers and scientists to help solve these problems.

OBJECTIVE

- The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
- The participant will be able to gather data, and determine how best to plot the data and make inferences from that data.
- The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
- The seminar offers a variety of video demonstrations of analysis techniques, so that the analyst can get an understanding of the types of results they might expect to see with their equipment.
- The participant will be able to identify basic test structures and how they are used to help quantify reliability on semiconductor devices.
- The participant will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
- The participant will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

WHO SHOULD ATTEND

Technical managers/engineers in Package/Wafer Level Reliability, Burn-In, Material & Process (M&P), QRA/failure analysis, R&D, Quality department, Product/Device Analysis, Package Development & anyone want to enhance knowledge in Package/Wafer level Reliability .

METHODOLOGY

Discussion and case study will provide participants with an indepth understanding of the subject matters and expose them with a real life situation.

DURATION

4 days

DATE & VENUE

26 - 29 June 2007 at SHRDC, Shah Alam

FEE

Normal Rate: RM4,900/participant

Group Discount (More than 6 participants) : RM4,000/participant

PSMB Scheme : SBL Khas

Please note that maximum claim under SBL Khas is RM1,000/pax/day.

Company has to pay the balance of the fee by cheque to SHRDC.

CONTACT INFO - Marketing Personnel (Kim Lai, Siti, Aizam or Pesala):



SHRDC

SELANGOR HUMAN RESOURCE DEVELOPMENT CENTRE

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WORLDWIDE BUSINESS COURSES

DAY 1

- Introduction to Reliability
 - Basic Concepts
 - Definitions
 - Historical Information
- Statistics and Distributions
 - Basic Statistics
 - Normal Distribution
 - Lognormal Distribution
 - Weibull Distribution
 - Exponential Distribution
 - Which Distribution Should I Use?
 - Data Handling

DAY 2

- Die-Level Failure Mechanisms
 - Time Dependent Dielectric Breakdown
 - Hot Carrier Damage
 - Negative Bias Temperature Instability
 - Electromigration
 - Stress Induced Voiding

DAY 3

- Package Level Mechanisms
 - Ionic Contamination
 - Moisture/Corrosion
 - Thermo-Mechanical Stress
 - Thermal Stress/Cycling
- Use Condition Mechanisms
 - Electrical Overstress/ESD
 - Radiation

DAY 4

- Test Structures and Test Equipment
 - Test Structures
 - Parametric Test Structures
 - Reliability Test Structures
 - Self-Stressing Test Structures
 - Test Equipment
 - Packaged Part Testing
 - Wafer Level Testing
- Developing Screens, Stress Tests, and Life Tests
 - Burn-In
 - Life Testing
 - HAST
- Package Attach (Solder) Reliability Mechanisms
- Board Level Reliability Mechanisms
- Calculating Chip and System Level Reliability
- Future Reliability Challenges

TRAINER BIODATA

Christopher L. Henderson - received his B.S in Physics from the New Mexico Institute of Mining and Technology and his M.S.E.E. from the University of New Mexico. Chris is the President and one of the founders of Semitracks Inc., a United States based company that provides education and training to the semiconductor industry. Chris also teaches courses in failure analysis, reliability and semiconductor technology for the semiconductor industry. From 1988 to 2004 he worked at Sandia National Laboratories, where he was a Principal Member of Technical Staff in the Failure Analysis Department and Microsystems Partnership Department. His job responsibilities have included failure and yield analysis of components fabricated at Sandia's Microelectronics Development Laboratory, research into the electrical behavior of defects, and consulting on microelectronics issues for the Department of Defense. He has published over 25 papers at various conferences in semiconductor processing, reliability, failure analysis and test. He has received two R&D 100 awards and two best paper awards. Prior to working at Sandia, Chris worked for Honeywell, BF Goodrich Aerospace, and Intel. Chris is a member of IEEE and EDFAS (the Electron Device Failure Analysis Society).

Publications & Articles:

- C. L. Henderson and J. M. Soden, "ICFAX, An Integrated Circuit Failure Analysis Expert System," Proceedings of the 1991 International Reliability Physics Symposium, April 1991, pp. 142-151.
- C. L. Henderson, J. M. Soden, and C. F. Hawkins, "The Behavior and Testing Implications of CMOS IC Logic Gate Open Circuits," Proceedings of the 1991 International Test Conference, October 1991, pp. 302-310.
- A. N. Campbell, E. I. Cole Jr., C. L. Henderson, and M. R. Taylor, "Case History: Failure Analysis of a CMOS SRAM with an Intermittent Open Contact," Proceedings of the 1991 International Symposium for Testing and Failure Analysis, November 1991, pp. 261-270.
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- C. L. Henderson, "Topics in Knowledge-Based Failure Analysis," Microelectronics Failure Analysis Desk Reference. 3rd Edition, ASM International, 1993, pp. 371-376.
- C. L. Henderson and D. L. Barton, "Advanced Failure Analysis Laboratory Equipment Networking", Proceedings of the IDS User's Conference, August 1993.
- C. L. Henderson and R. D. Barnard, "The Advent of Failure Analysis Software Technology", Proceedings of IEEE International Reliability Physics Symposium, April 11-14, 1994, pp. 325-333.
- E. I. Cole Jr., Jerry M. Soden, James L. Rife, Daniel L. Barton, and Christopher L. Henderson, "Novel Failure Analysis Techniques Using Photon Probing With a Scanning Optical Microscope", Proceedings of IEEE International Reliability Physics Symposium, April 11-14, 1994, pp. 388-398.
- R. E. Anderson, J. M. Soden and C. L. Henderson, "Failure Analysis: Status and Future Trends", International Workshop on Semiconductor Characterization: Present Status and Future Needs, National Institute of Standards and Technology (NIST, Gaithersburg, MD), Jan. 30-Feb. 2, 1995, (Published in book, Semiconductor Characterization: Present Status and Future Needs, AIP Press, 1996, pp. 187-196)
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- J. M. Soden, R. E. Anderson, and C. L. Henderson, "IC Failure Analysis Tools and Techniques—Magic Mystery and Science", International Test Conference, Lecture Series 2, October 1996.
- C. L. Henderson and J. M. Soden, "A Signature Analysis Method for IC Failure Analysis", International Symposium for Testing and Failure Analysis (ISTFA), November 1996.
- C. L. Henderson, J. M. Soden, and R. E. Anderson, "Yield and Failure Analysis Challenges in IC Manufacturing", Future Fab International, Volume 1, Issue 2 (1997) pp. 335-343.
- J. M. Soden and C. L. Henderson, "IC Diagnosis: Industry Trends", International Test Conference, p. 435, November 1997.
- J. M. Soden, R. E. Anderson, and C. L. Henderson, "IC Failure Analysis: Magic Mystery and Science", IEEE Design and Test of Computers, Vol. 14, No. 3, July-Sept. 1997, pp. 59-69.
- C. L. Henderson and J. M. Soden, "Signature Analysis for IC Diagnosis and Failure Analysis", International Test Conference, pp. 310-318, Nov. 1997.
- E. I. Cole, J. M. Soden, P. Tangyungyong, P. Candelaria, R. W. Beegle, D. L. Barton, C. L. Henderson, and C. F. Hawkins, "Transient Power Supply Voltage (VDDT) Analysis for Detecting IC Defects", International Test Conference, pp. 23-31, November 1997.
- C. L. Henderson, C. E. Hembree, J. M. Soden, T. J. Headley, and B. L. Draper, "Identification of Yield Limited Defects in a 0.5 Micron, Shallow Trench Isolation Technology," International Symposium for Testing and Failure Analysis, November 1999, pp. 405-412.
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- C. L. Henderson, "Failure Analysis Terms and Definitions," Microelectronics Failure Analysis Desk Reference 4th Edition, ASM International, 1999, pp. 603-614.
- C. L. Henderson, D. L. Barton, E. I. Cole Jr., and M. P. Strizich, 21st Century Product Analysis Handbook, Semitracks Inc., 2001-2005.
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- C. L. Henderson, "Education and Training for the Analyst," Electronic Device Failure Analysis, Vol. 5, No. 1, pp. 5-9, Feb. 2003.
- C. L. Henderson, "Failure Analysis - Fundamentals and Advanced Techniques for Nanotechnology," 2005 Reliability Physics Tutorial Notes, pp. 131.1-52, 2005.

Registration Form

Fax to:
(03) 5513 3490



SHRDC

Title **Advanced Semiconductor Package/Wafer Reliability**

Date **26 - 29 June 2007, SHRDC Shah Alam**

Company Name

Address

Contact Person

Tel No.

Fax No.

Email

Details of Participant(s)

No	Participant's Full Name	Designation	Department	New I.C. No
1				
2				
3				
4				
5				

Approved By

Signature

Date

Full Name

Designation

Company Stamp/Chop

For further information, please contact our Marketing Personnel (Kim Lai, Siti, Aizam or Pesala) at

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